Amendments to the Claims

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Previously Presented) A method for verifying an integrated circuit device test for testing an integrated circuit device, said method comprising the steps of:

simulating a flawed integrated circuit device design comprising a good integrated circuit design modified to include one or more known physical flaws in the good integrated circuit device design;

simulating said integrated circuit device test to test said simulated flawed integrated circuit device design; and

determining whether said simulated test of said simulated flawed integrated circuit device design discovered said one or more known physical flaws in said simulated flawed integrated circuit device design.

2. (Canceled)

3. (Currently Amended) The method of claim [[3]] 1, further comprising the step of:

indicating that said integrated circuit device test is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover said one or more known physical flaws in said simulated flawed integrated circuit device design.

4. (Previously Presented) The method of claim 1, further comprising the step of:

indicating that said integrated circuit device test is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover

said one or more known physical flaws in said simulated flawed integrated circuit device design.

5. (Previously Presented) The method of claim 1, further comprising the step of:

simulating said good integrated circuit device design.

6. (Previously Presented) The method of claim 5, further comprising the step of:

simulating said integrated circuit device test to test said simulated good integrated circuit device design; and

indicating that said integrated circuit device test is flawed if said simulated test of said simulated good integrated circuit device design does not pass.

7. (Previously Presented) The method in accordance with claim 6, wherein:

the flawed integrated circuit device design comprises the good integrated circuit device design modified to include the one or more known physical flaws.

8. (Previously Presented) The method of claim 7, further comprising the step of:

indicating that said integrated circuit device test is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover said one or more known physical flaws in said simulated flawed integrated circuit device design.

9. (Previously Presented) The method of claim 1, comprising the step of:

modifying said good integrated circuit device design to include said one or more known physical flaws to generate said flawed integrated circuit device design.

10. (Canceled)

11. (Canceled)

12. (Previously Presented) The method of claim 9, further comprising the step of:

indicating that said integrated circuit device test is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover said one or more known physical flaws in said simulated flawed integrated circuit device design.

13. (Previously Presented) The method of claim 9, further comprising the first step of:

simulating said good integrated circuit device design.

14. (Previously Presented) The method of claim 13, further comprising the step of:

simulating said integrated circuit device test to test said simulated good integrated circuit device design; and

indicating that said integrated circuit device test is flawed if said simulated test of said simulated good integrated circuit device design does not pass.

15. (Previously Presented) The method of claim 14, wherein:

the flawed integrated circuit device design comprises the good integrated circuit device design modified to include the one or more known physical flaws.

16. (Previously Presented) The method of claim 15, further comprising the step of:

indicating that said integrated circuit device test is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover

said one or more known physical flaws in said simulated flawed integrated circuit device design.

17. (Previously Presented) A computer readable storage medium tangibly embodying program instructions implementing a method for verifying an integrated circuit device test for testing an integrated circuit device, said method comprising the steps of:

simulating a flawed integrated circuit device design comprising a good integrated circuit design modified to include one or more known physical flaws in the good integrated circuit device design;

simulating said integrated circuit device test to test said simulated flawed integrated circuit device design; and

determining whether said simulated test of said simulated flawed integrated circuit device design discovered said one or more known physical flaws in said simulated flawed integrated circuit device design.

18. (Canceled)

19. (Previously Presented) The computer readable storage medium of claim 17, further comprising the step of:

indicating that said integrated circuit device test is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover said one or more known physical flaws in said simulated flawed integrated circuit device design.

20. (Previously Presented) The computer readable storage medium of claim 17, further comprising the step of:

indicating that said integrated circuit device test is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover said one or more known physical flaws in said simulated flawed integrated circuit device design.

21. (Previously Presented) The computer readable storage medium of claim 17, further comprising the first step of:

simulating said good integrated circuit device design.

22. (Previously Presented) The computer readable storage medium of claim 21, further comprising the step of:

simulating said integrated circuit device test to test said simulated good integrated circuit device design; and

indicating that said integrated circuit device test is flawed if said simulated test of said simulated good integrated circuit device design does not pass.

23. (Previously Presented) The computer readable storage medium of claim 22, wherein:

the flawed integrated circuit device design comprises the good integrated circuit device design modified to include the one or more known physical flaws.

24. (Previously Presented) The computer readable storage medium of claim 23, further comprising the step of:

indicating that said integrated circuit device test is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover said one or more known physical flaws in said simulated flawed integrated circuit device design.

25. (Previously Presented) The computer readable storage medium of claim 17, comprising the step of:

modifying said good integrated circuit device design to include said one or more known flaws to generate said flawed integrated circuit device design.

26. (Canceled)

27. (Canceled)

28. (Previously Presented) The computer readable storage medium of claim 25, further comprising the step of:

indicating that said integrated circuit device test is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover said one or more known physical flaws in said simulated flawed integrated circuit device design.

29. (Previously Presented) The computer readable storage medium of claim 25, further comprising the step of:

simulating said good integrated circuit device design.

30. (Previously Presented) The computer readable storage medium of claim 29, further comprising the step of:

simulating said integrated circuit device test to test said simulated good integrated circuit device design; and

indicating that said integrated circuit device test is flawed if said simulated test of said simulated good integrated circuit device design does not pass.

31. (Previously Presented) The computer readable storage medium of claim 30, wherein:

the flawed integrated circuit device design comprises the good integrated circuit device design modified to include the one or more known physical flaws.

32. (Previously Presented) The computer readable storage medium of claim 31, further comprising the step of:

indicating that said integrated circuit device test is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover said one or more known physical flaws in said simulated flawed integrated circuit device design.

33. (Previously Presented) An integrated circuit device test verification apparatus, comprising:

an integrated circuit device simulator which simulates a flawed integrated circuit device design, said flawed integrated circuit device design comprising a good integrated circuit design modified to include one or more known physical flaws in the good integrated circuit device design;

a tester simulator which simulates an integrated circuit device test executing on an integrated circuit device tester that generates test stimuli, applies said generated test stimuli to said simulated flawed integrated circuit device design, and receives test responses from said simulated flawed integrated circuit device design; and

a simulated test results analyzer which determines whether said simulated integrated circuit device test of said simulated flawed integrated circuit device design discovered said one or more known physical flaws in said flawed integrated circuit device design.

34. (Canceled)

35. (Previously Presented) The integrated circuit device test verification apparatus of claim 33, wherein:

said simulated test results analyzer determines that said integrated circuit device test is flawed if said simulated test of said simulated flawed integrated circuit device design does not discover said one or more known physical flaws in said simulated flawed integrated circuit device design.

36. (Previously Presented) The integrated circuit device test verification apparatus of claim 33, wherein:

said integrated circuit device simulator also simulates said good integrated circuit device design;

said tester simulator simulates said integrated circuit device test executing on said integrated circuit device tester, and applies said generated test stimuli to said simulated good integrated circuit device design, and receives test responses from said simulated good integrated circuit device design; and

said simulated test results analyzer determines whether said simulated test of said simulated good integrated circuit device design passes said simulated good integrated circuit device design.

37. (Previously Presented) The integrated circuit device test verification apparatus of claim 36, wherein:

said simulated test results analyzer determines that said integrated circuit device test is flawed if said simulated test of said simulated good integrated circuit device design does not pass said simulated good integrated circuit device design.